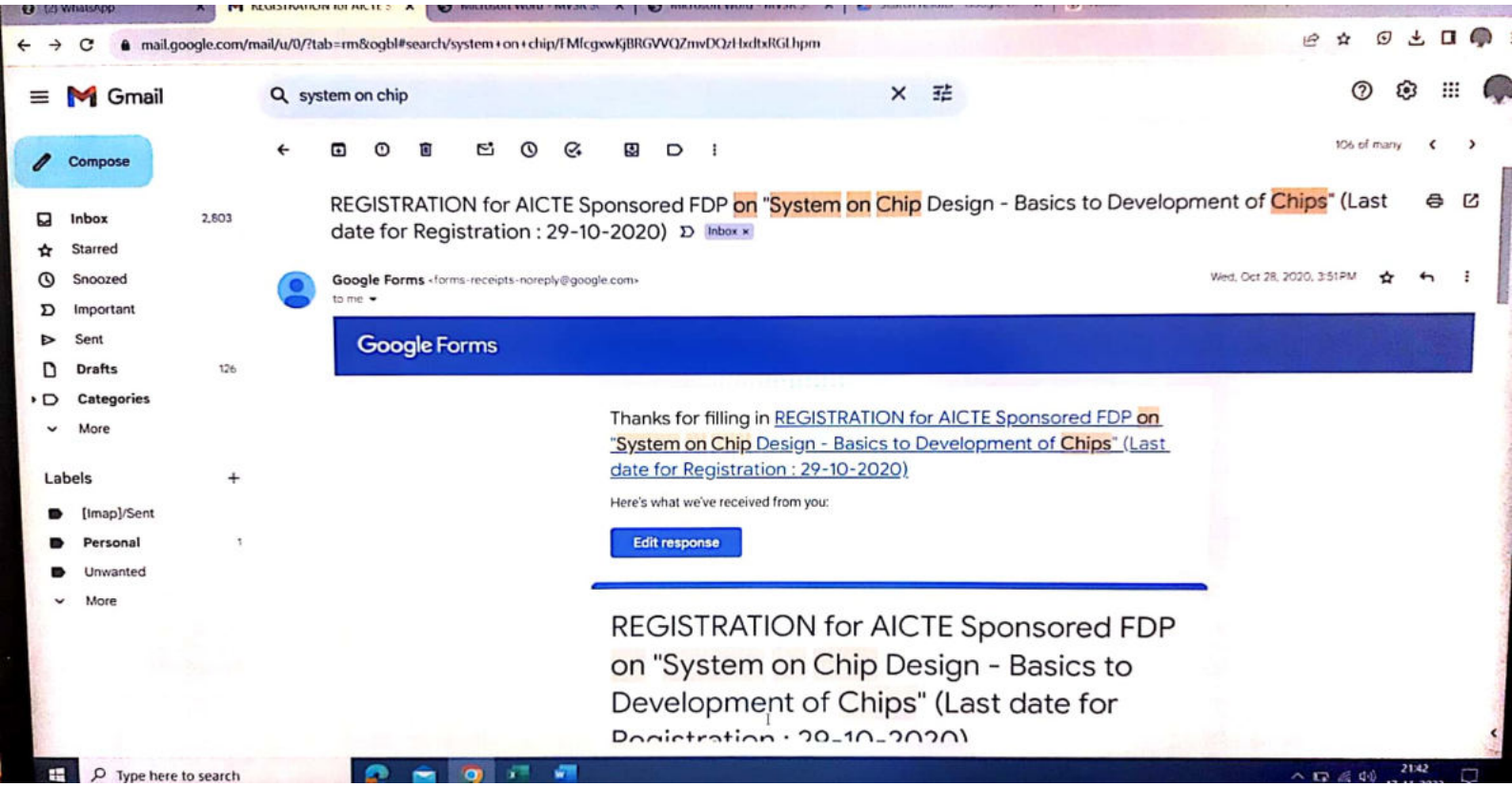

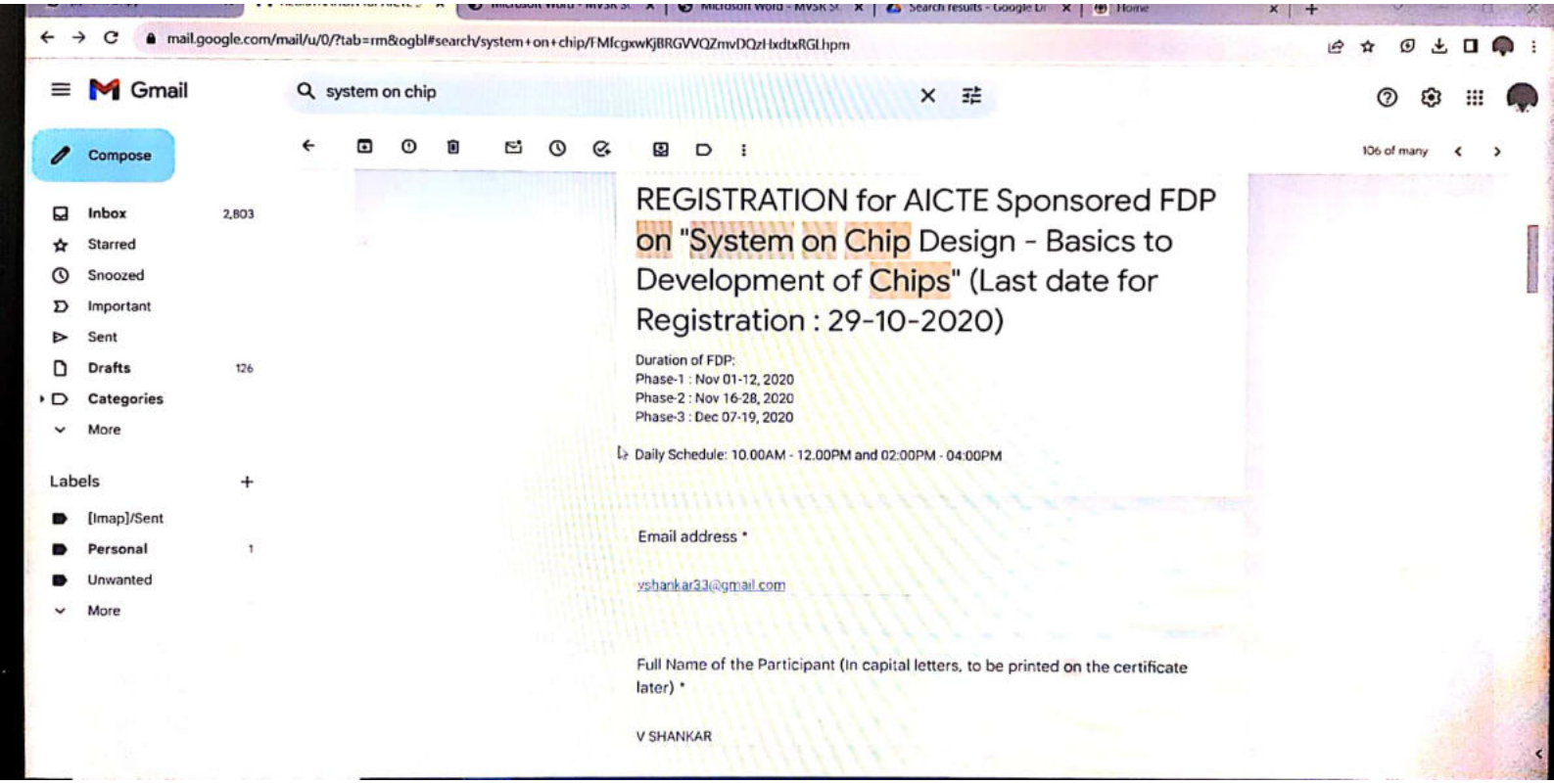

Full Name of the Participant (In capital letters, to be printed on the certificate later) *

V SHANKAR

Highest Qualification *

- ○ B.E/B.Tech
- ◉ M.E/M.Tech/M.S
- ○ Ph.D
- ○ Other:

Designation *

- ○ Lecturer
- ◉ Assistant Professor
- ○ Associate Professor
- ○ Professor

Designation *

- ○ Lecturer
- ◉ Assistant Professor
- ○ Associate Professor
- ○ Professor
- ○ Other: _____

Name of the Institution/Organization (Write full name, to be printed on the certificate later) *

G NARAYANAMMA INSTITUTE OF TECHNOLOGY & SCIENCE(For Women)

AICTE ID of Institute (Link: https://www.aicte-india.org/downloads/Institute_List.pdf)

Maturi Venkata Subba Rao (MVSR) Engineering College, Nadergul, Hyderabad-501510

Department of Electronics and Communication Engineering

Dear Sir/ Madam

Greetings from the Department of ECE, Maturi Venkata Subba Rao (MVSR) Engineering College!

Your name has been nominated to attend the two weeks FDP ***System on Chip Design Basics to Development of Chips*** which is sponsored by AICTE.

Duration: Two weeks
Dates: 1st to 12th November 2020

Details regarding the conduct of FDP will be shared in the following Whatsapp group.

https://chat.whatsapp.com/ChoUm0rbtjGBvL8GFf13VB

Kindly note the following:

1. Attendance will be monitored during all the sessions.
2. Login 15 minutes in advance, so that we can start the session right on time.
3. Keep your microphone and video muted always.
4. If you have any question, put in the chat box when the session is about to complete.
5. After the presentation of the speaker you can un-mute and ask questions to the speaker through the session coordinator.
6. Kindly cooperate in smooth conduction of all sessions and FDP.

Note: FDP will be conducted as per guidelines of AICTE.

For any queries please contact Mr. Mahendar Gajula, 9059364420.

Best wishes!

Dr. S.P. Venu Madhava Rao
Co-ordinator AICTE-FDP
Head
Department of ECE,
MVSR Engineering College.

MATURI VENKATA SUBBA RAO (MVSR) ENGINEERING COLLEGE

(Sponsored by Matrusri Education Society, Estd. 1980)

Affiliated to Osmania University & Approved by AICTE

Nadergul, Hyderabad - 501 510.

Department of Electronics and Communication Engineering

Certificate of Participation

This is to certify that

Mr. V. Shankar, Asst. Prof.,

of **G. Narayanamma Instiute of Technology & Science for Women**

has participated in two week AICTE sponsored FDP on

System on Chip Design - Basics to Development of Chips

from 1st - 12th November, 2020.

S.P. Venu Madhava Rao

Dr. S.P. Venu Madhava Rao
Co-ordinator

Dr. G. Kanaka Durga
Principal

NBA Accredited Courses Civil,CSE,ECE, EEE,Mech & IT

ACCREDITED BY NAAC

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