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Courses » Switching Circuits and Logic Design

Course outline

Switching Circuits and Logic Design

ABOUT THE COURSE:

This course will discuss the basic background of switching circuits, and discuss techniques for mapping the theory to actual hardware circuits. Synthesis and minimization techniques of combinational and sequential circuits shall be discussed in detail. Designing circuits using high-level functional blocks shall also be discussed. The course will closely follow the undergraduate curriculum existing in most engineering colleges.

Important For Certification/Credit Transfer:

Weekly Assignments and Discussion Forum can be accessed ONLY by enrolling here

Scroll down to Enroll

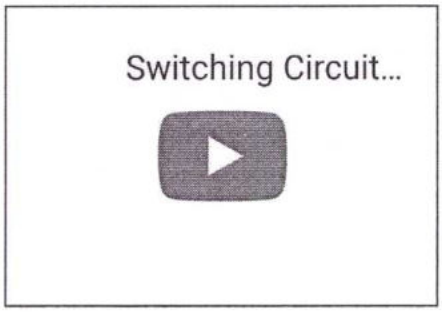
Note: Content is Free!

All content including discussion forum and assignments, is free

Final Exam (in-person, invigilated, currently conducted in India) is mandatory for Certification and has INR Rs. 1100 as exam fee

INTENDED AUDIENCE:

Computer Science and Engineering / Information Technology / Electronics and Communication Engineering / Electrical Engineering



6572 students have enrolled already!!

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G. Narayanamma Institute of Technology & Science (for women)
(AUTONOMOUS)
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CORE/ELECTIVE: Elective

UG/PG: UG

PREREQUISITES: Basic knowledge of electronics and electrical circuitsl

INDUSTRY SUPPORT: TCS, Wipro, CTS, Google, Microsoft, HP, Intel, IBM

ABOUT THE INSTRUCTOR:

Prof. IndranilSengupta has obtained his B.Tech.,M.Tech. and Ph.D. degrees in Computer Science and Engineering (CSE) from the University of Calcutta. He joined the Indian Institute of Technology, Kharagpur, as a faculty member in 1988, in the Department of CSE, where he is presently a full Professor. He had been the former Heads of the Department of Computer Science and Engineering and also the School of Information Technology of the Institute. He has over 28 years of teaching and research experience. He has guided 22 PhD students, and has more than 200 publications to his credit in international journals and conferences. His research interests include reversible and quantum computing, VLSI design and testing, and information security.
He is a Senior Member of IEEE. He had been the General Chairs of Asian Test Symposium (ATS-2005), International Conference on Cryptology in India (INDOCRYPT-2008), International Symposium on VLSI Design and Test (VDAT-2012), International Symposium on Electronic System Design (ISED-2012), and the Conference on Reversible Computation (RC-2017).

COURSE LAYOUT:

Week 1 : Introduction to number systems and codes, error detection and correction, binary arithmetic.
Week 2 : Switching primitives and logic gates, logic

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families: TTL, CMOS, memristors, all-optical realizations.
Week 3 : Boolean algebra: Boolean operations and functions, algebraic manipulation, minterms and maxterms, sum-of-products and product-of-sum representations, functional completeness.
Week 4 : Minimization of Boolean functions: K-map method, prime implicants, don't care conditions, Quine-McCluskey method, multi-level minimization.
Week 5 : Design of combinational logic circuits: adders and subtractors, comparator, multiplexer, demultiplexer, encoder, etc.
Week 6 : Representation of Boolean functions: binary decision diagram, Shannon's decomposition, Reed-Muller canonical form, etc.
Week 7 : Design of latches and flip-flops: SR, D, JK, T. Master-slave and edge-triggered flip-flops. Clocking and timing issues.
Week 8 : Synthesis of synchronous sequential circuits, Mealy and Moore machines, state minimization.
Week 9 : Design of registers, shift registers, ring counters, binary and BCD counters. General counter design methodology.
Week 10 : Algorithmic state machine and data/control path design.
Week 11 : Asynchronous sequential circuits: analysis and synthesis, minimization, static and dynamic hazards.
Week 12 : Testing and fault diagnosis in digital circuits: fault modeling, test generation and fault simulation, fault diagnosis, design for testability and built-in self-test.

SUGGESTED READING MATERIALS:

1.ZviKohavi and Niraj K. Jha, "Switching and Finite Automata Theory", 3rd Edition, Cambridge University Press, 2010.
2.M. Morris Mano and Michael D. Ciletti, "Digital Design: With an Introduction to the Verilog HDL", 5th Edition, Pearson Education, 2013.
3.Randy H. Katz and Gaetano Borriello, "Contemporary Logic Design", 2nd Edition, Pearson Education, 2005.

CERTIFICATION EXAM :

- The exam is optional for a fee.
- Date and Time of Exam: **October 28, 2018 (Sunday)**:
- Time of Exams: **Morning session 9am to 12 noon; Afternoon session: 2pm to 5pm.**
- Exam for this Course will be available in **both morning & afternoon sessions.**
- Registration url: Announcements will be made when the registration form is open for registrations.
- The online registration form has to be filled and the certification exam fee needs to be paid. More details will be made available when the exam registration form is published.

CERTIFICATE:

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- Final score will be calculated as : 25% assignment score + 75% final exam score
- 25% assignment score is calculated as 25% of average of Best 8 out of 12 assignments
- E-Certificate will be given to those who register and write the exam and score greater than or equal to 40% final score. Certificate will have your name, photograph and the score in the final exam with the breakup.It will have the logos of NPTEL and IIT Kharagpur.It will be e-verifiable at http://nptel.ac.in/noc/

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Roll No:NPTEL18CS30S11391006

To

GUNDRALA MADHAVI
H.NO:4-4-49/320,ABHYUDHAYA NAGAR
COLONY,KALIMANDIR
BANDLAGUDA,DONBOSCO
HYDERABAD
TELANGANA
500086
PH. NO :9676388078

Score	Type of Certificate
>=90	Elite + Gold Medal
60-89	Elite
40-59	Successfully Completed the course
<40	No Certificate

No. of credits recommended by NPTEL:3

Elite

NPTEL Online Certification

(Funded by the Ministry of HRD, Govt. of India)

This certificate is awarded to

GUNDRALA MADHAVI

for successfully completing the course

Switching Circuits and Logic Design

with a consolidated score of **70** %

Online Assignments	23.34/25	Proctored Exam	46.5/75

Total number of candidates certified in this course: **723**

Prof. Anupam Basu
NPTEL Coordinator
IIT Kharagpur

Jul-Oct 2018
(12 week course)

A. Goswami
Prof. Adrijit Goswami
Dean
Continuing Education, IIT Kharagpur

Indian Institute of Technology Kharagpur

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Department: Electronics and Communication Engineering
2018-19
REPORT
NPTEL FDP on "**Switching Circuits and Logic Design**"

Date of program: 26 July 2018- 15 Oct 2018
Resource person: Prof. Indranil Sengupta
About the Program:

This course will give the basic background of switching circuits and techniques for mapping the theory to actual hardware circuits. Synthesis and minimization techniques of combinational and sequential circuits shall be discussed in detail.

Week 1: Introduction to number systems and codes, error detection and correction, binary arithmetic.
Week 2: Switching primitives and logic gates, logic families: TTL, CMOS, memristors.
Week 3: Boolean algebra: Boolean operations and functions, algebraic manipulation, minterms and maxterms, sum-of-products and product-of-sum representations, functional completeness.
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Week 6: Representation of Boolean functions: binary decision diagram, Shannon's decomposition, Reed-Muller canonical form, etc.

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Week 10: Algorithmic state machine and data/control path design.
Week 11: Asynchronous sequential circuits: analysis and synthesis, minimization, static and dynamic hazards.
Week 12: Testing and fault diagnosis in digital circuits: fault modeling, test generation and fault simulation, fault diagnosis, design for testability and built-in self-test.
The overall experience helpful in understanding the concepts of combinational circuits and Testing and fault diagnosis in digital circuits

Signature of the Faculty member

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