Brief Summary

FDP on – Trends in reconfigurable (FPGA) SoC Design

From 25th Dec to 30th Dec

2018 Sponsored by

Electronics &ICT academy

Organized by

Department of Electronics & Communication Engineering,

National Institute Of technology, Warangal.

The objective of this Faculty Development Program (FDP) is to motivate the faculty participants of different colleges to enhance the class room subject delivery and also to improve the research and innovation of faculty in the area of new trends of Satellite Communication systems.This one-week FDP on "Trends in Reconfigurable (FPGA) SoC design" offered an expert view on availability of powerful, low costand less weight CMOS system design.

The inaugural session was presided by Dr. B.Bheema Rao HOD and Program Coordinator Muralidhar on sunday, 25th Dec 2018., assistant director jay Kumar NIT warangal ,Mr. Srinivas Reddy Kotta, was the chief guest of the inaugural function.

During these six days faculty development program, eminent speakers from Intel ,DRDO, AMD, NIT Warangal and Technical experts from Core-el were invited to share their knowledge and expertise. Within a span of six day, ten informative technical talks and four training sessions by industry representatives were conducted on SoC and Zinq board . It was very great experience for faculty.

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cation Systems,FDPwas inaugurated by our **Chief Guest Prof. G M Patil**, Principal, JSSATE, Noida on Monday, 7th May 2018 at 9:30AM.

Cmde B. K. Gupta, CAO was the chief guest for the FDP - Next Generation Nano Satellite Communication Systems, valedictory session held on Friday,11th May 2018 at 3.00PM.

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Ministry of Electronics and Information Technology
Government of India

ELECTRONICS & ICT ACADEMY

NATIONAL INSTITUTE OF TECHNOLOGY WARANGAL, (T.S.), INDIA

and

Department of Electronics and Communication Engineering, NITW

Participation Certificate

This is to certify that V Shankar, Assistant Professor

from G. Narayanamma Institute of Technology and Science

has participated in MeitY, Govt. of India, Sponsored One Week Faculty Development Programme (FDP) on "Trends in Reconfigurable (FPGA) SoC Design" Organized by the E & ICT Academy, National Institute of Technology, Warangal at Department of ECE, NIT, Warangal from 25th -30th November, 2018.

Participant performance is satisfactory.

Dr. P. Muralidhar	Dr. MD. Farukh Hashmi	Prof.N.Bheema Rao	Prof. D.V.L.N. Somayajulu	Prof. N.V. Ramana Rao
Coordinator, Dept. of ECE, NITW	Coordinator, Dept. of ECE, NITW	HOD, Dept. of ECE, NITW	Chair, E & ICT Academy, NIT, Warangal	Director, NIT, Warangal

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REPORT

Department: Electronics and Communication Engineering

2018-19

FDP on "FDP on Trends in Reconfigurable (FPGA) SOC Design

Date of program: 25-11-2018 to 30-11-2018

Resource Persons:
Dr. MD Farukh Hashmi, Assistant Professor, NIT Warangal
Dr. P. Muralidhar, Associate Professor, NIT Warangal
r. B. Lakshmi, Associate Professor, NIT Warangal
Prof. T. Kishore Kumar, Professor, NIT Warangal
Dr. Narendra Vadthiya, Assistant Professor, NIT Warangal
Prof. N. S. Murthy, Professor, Vasavi College of Engineering, Hyderabad
Dr. P. Sreehari Rao, Associate Professor, NIT Warangal
Mr. M. V. Krishna Reddy, Texas Instruments, Bangalore
Dr. Anand Babu, DRDO, Hyderabad
Mr. Venkateswara Rao, AMD, India
Mr. S. Rama Krishna, Intel, Bangalore
Dr. Nagendra Bandi, Application Engineer, Correel Tech, Hyderabad
Mr. K. Srinivas Reddy, Ideabytes Ltd, Hyderabad

About the Program:

The FDP was organised from 25th Nov 2018 to 30th Nov 2018. The first day FN and AN sessions by Dr.MD Farukh Hashmi, Assistant Professor, NIT Warangal and Dr. P Muralidhar, Associate Professor, NIT Warangal on Trends in SoC design and image sensor SoC and the session was excellent. On the second day of the FDP, FN session was by Dr. B Lakshmi, Assistant. Prof, ECE Dept, NITW on Introduction to Verilog HDL followed by a hands-on session on Vivado tool and Narendra Vadthya on the SoC technology. Third day was on low power VLSI architecture and hardware software co Design and processor design. Fourth day of the FDP, FN session was N.S Murthy Prof, Vasavi Engineering college Hyderabad. Fifth was a session by M.V Krishna Murthy on Zinq board and followed by hands on session. 6th day was a session on Introduction to current trends in technology by Venkateshwara Rao, AMD India and AN session on Reconfigurable on SoC system processor by Nagendra Bandi Application Engineer,Correel Technology,Hyderabad.

The overall experience of attending the workshop is quite helpful in a better understanding on Zinqs boards, concept on system on chip and how to apply in the field of VLSI and low power VLSI design.

- FDP was very informative, useful and research oriented.
- Organization of the FDP was good.
- Resource Persons are the major Highlight of the programme.

Signature of the Faculty member

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