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Switching Circuits and Logic Design

This course will discuss the basic background of switching circuits, and discuss techniques for mapping the theory to actual hardware circuits. Synthesis and minimization techniques of combinational and sequential circuits shall be discussed in detail. Designing circuits using high-level functional blocks shall also be discussed. The course will closely follow the undergraduate curriculum existing in most engineering colleges.

INTENDED AUDIENCE: Any Engineering Students/Faculty
PREREQUISITES: Basic knowledge of electronics and electrical circuitsl
INDUSTRY SUPPORT: TCS, Wipro, CTS, Google, Microsoft, HP, Intel, IBM

Prof. Indranil Sengupta has obtained his B.Tech.,M.Tech. and Ph.D. degrees in Computer Science and Engineering (CSE) from the University of Calcutta. He joined the Indian Institute of Technology, Kharagpur, as a faculty member in 1988, in the Department of CSE, where he is presently a full Professor. He had been the former Heads of the Department of Computer Science and Engineering and also the School of Information Technology of the Institute. He has over 28 years of teaching and research experience. He has guided 22 PhD students, and has more than 200 publications to his credit in international journals and conferences. His research interests include reversible and quantum computing, VLSI design and testing, and information security.

He is a Senior Member of IEEE. He had been the General Chairs of Asian Test Symposium (ATS-2005), International Conference on Cryptology in India (INDOCRYPT-2008), International

Symposium on VLSI Design and Test (VDAT-2012), International Symposium on Electronic System Design (ISED-2012), and the Conference on Reversible Computation (RC-2017).

COURSE TYPE

Elective

COURSE LEVEL

Undergraduate

COURSE LAYOUT

Week 1 : Introduction to number systems and codes, error detection and correction, binary arithmetic.
Week 2 : Switching primitives and logic gates, logic families: TTL, CMOS, memristors, all-optical realizations.
Week 3 : Boolean algebra: Boolean operations and functions, algebraic manipulation, minterms and maxterms, sum-of-products and product-of-sum representations, functional completeness.
Week 4 : Minimization of Boolean functions: K-map method, prime implicants, don't care conditions, Quine-McCluskey method, multi-level minimization.
Week 5 : Design of combinational logic circuits: adders and subtractors, comparator, multiplexer, demultiplexer, encoder, etc.
Week 6 : Representation of Boolean functions: binary decision diagram, Shannon's decomposition, Reed-Muller canonical form, etc.
Week 7 : Design of latches and flip-flops: SR, D, JK, T. Master-slave and edge-triggered flip-flops. Clocking and timing issues.
Week 8 : Synthesis of synchronous sequential circuits, Mealy and Moore machines, state minimization.
Week 9 : Design of registers, shift registers, ring counters, binary and BCD counters. General counter design methodology.
Week 10: Algorithmic state machine and data/control path design.
Week 11: Asynchronous sequential circuits: analysis and synthesis, minimization, static and dynamic hazards.
Week 12: Testing and fault diagnosis in digital circuits: fault modeling, test generation and fault simulation, fault diagnosis, design for testability and built-in self-test.

BOOKS AND REFERENCES

1.ZviKohavi and Niraj K. Jha, "Switching and Finite Automata Theory", 3rd Edition, Cambridge University Press, 2010.

2.M. Morris Mano and Michael D. Ciletti, "Digital Design: With an Introduction to the Verilog HDL", 5th Edition, Pearson Education, 2013.
3.Randy H. Katz and Gaetano Borriello, "Contemporary Logic Design", 2nd Edition, Pearson Education, 2005.

CERTIFICATE

- The course is free to enroll and learn from. But if you want a certificate, you have to register and write the proctored exam conducted by us in person at any of the designated exam centres.
- The exam is optional for a fee of Rs 1000/- (Rupees one thousand only).
- **Date and Time of Exams: 16 November 2019,** Morning session 9am to 12 noon; Afternoon Session 2pm to 5pm.
- Registration url: Announcements will be made when the registration form is open for registrations.
- The online registration form has to be filled and the certification exam fee needs to be paid. More details will be made available when the exam registration form is published. If there are any changes, it will be mentioned then.
- Please check the form for more details on the cities where the exams will be held, the conditions you agree to when you fill the form etc.

CRITERIA TO GET A CERTIFICATE

- Average assignment score = 25% of average of best 8 assignments out of the total 12 assignments given in the course.
- Exam score = 75% of the proctored certification exam score out of 100
- Final score = Average assignment score + Exam score

YOU WILL BE ELIGIBLE FOR A CERTIFICATE ONLY IF AVERAGE ASSIGNMENT SCORE >=10/25 AND EXAM SCORE >= 30/75.

- If one of the 2 criteria is not met, you will not get the certificate even if the Final score >= 40/100.
- Certificate will have your name, photograph and the score in the final exam with the breakup.It will have the logos of NPTEL and IIT Kharagpur. It will be e-verifiable at nptel.ac.in/noc (http://nptel.ac.in/noc).
- Only the e-certificate will be made available. Hard copies are being discontinued from July 2019 semester and will not be dispatched

PRINCIPAL
G. Narayanamma Institute of
Technology & Science (for women)
(AUTONOMOUS)
Shaikpet, Hyderabad - 500 104

Roll No:NPTEL19CS74S41471949

To SREEKANTH REDDY BODEDDULA
50208, INDU FORTUNE FIELDS GARDENIA,
PHASE XIII, KPHB COLONY
HYDERABAD
TELANGANA
500085
PH. NO :9492036284

No. of weeks of NPTEL Courses	Equivalence of NPTEL course with regular FDP
4	$\frac{1}{2}$ FDP of one week
8	Full FDP of one week
12	$1\frac{1}{2}$ FDP

Duration of NPTEL course: 12 Weeks

NPTEL-AICTE
Faculty Development Programme

(Funded by the Ministry of HRD, Govt. of India)

This certificate is awarded to

SREEKANTH REDDY BODEDDULA

for successfully completing the course

Switching Circuits and Logic Design

with a consolidated score of **85** %

Prof. Andrew Thangaraj
NPTEL Coordinator
IIT Madras

(Jul-Oct 2019)

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Prof. Dileep N. Malkhede
Advisor-I (Research, Institute & Faculty Development)
All India Council for Technical Education

Roll No: NPTEL19CS74S41471949

To validate and check scores: http://nptel.ac.in/noc

The candidate has studied the above course through MOOCs mode, has submitted online assignments and passed proctored exams.
This certificate is therefore acceptable for promotions under CAS as per AICTE notifications dated 24th July 2018, similar to other refresher / orientation courses.
F.No. AICTE / RIFD / FDP through MOOCs / 2017-18

G.NARAYANAMMA INSTITUTE OF TECHNOLOGY & SCIENCE (For Women)
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Department: Electronics and Communication Engineering
2019-20
REPORT
NPTEL FDP on "**Switching Circuits and Logic Design**"

Date of Program: 29 July 2019 – 18 October 2019
Resource Person: Prof. Indranil Sen Gupta, IIT Kharagpur

About the Program:

This course discussed the basic background of switching circuits, and the techniques for mapping the theory to actual hardware circuits. Synthesis and minimization techniques of combinational and sequential circuits were discussed in detail. Designing circuits using high-level functional blocks was also discussed.

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Signature of the Faculty member

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